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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

LEWIS, MONICA

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 12/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/015,847

Applicant(s)

LETAVIC ET AL.

Examiner

Monica Lewis

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 November 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 December 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the election filed November 25, 2002.

Election/Restrictions

2. Applicant's election of Group I in Paper No. 6 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

4. The drawings are objected to because it is not clear as whether "Related Art" is "Prior Art." Therefore, if figures 1 and 2 are prior art please label them as such. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by the following: a) "and wherein a decrease of approximately 30% for a specific on resistance of the device.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-5, 7-9 and 11 are rejected under 35 U.S.C. 103(a) as obvious over Merchant (U.S. Patent No. 5,412,241) in view of Applicant's Related Art.

In regards to claim 1, Merchant discloses the following:

Figure 1);

- a) a buried oxide layer (2) formed over a semiconductor substrate (3) (See Figure 1);
- b) a silicon layer (1) formed over the buried oxide layer (See Figure 1);
- c) a top oxide layer (6) formed over the silicon layer (See Figure 1); and
- d) a first gate oxide (8) formed over the silicon layer adjacent the top oxide layer.

In regards to claim 1, Merchant fails to disclose the following:

- a) a second gate oxide formed over a portion of the first gate oxide.

However, Applicant's Related Art discloses a second gate oxide (50) over a portion of the first gate oxide (44) (See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a second gate oxide as disclosed in Applicant's Related Art because it aids in increasing the breakdown voltage.

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Additionally, since Merchant and Applicant's Related Art are both from the same field of endeavor, the purpose disclosed by Applicant's Related Art would have been recognized in the pertinent art of Merchant.

In regards to claim 2, Merchant discloses the following:

a) the silicon layer comprises a source region (10), a body region (9), and a drift region (4) (See Figure 1).

In regards to claim 3, Merchant discloses the following:

a) the first gate oxide is formed over the drift region, the body region, and the source region (See Figure 1).

In regards to claim 4, Merchant discloses the following:

a) the first gate oxide, top oxide layer and the body region (See Figure 1).

In regards to claim 4, Merchant fails to disclose the following:

a) a second gate oxide.

However, Applicant's Related Art discloses a second gate oxide (See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a second gate oxide as disclosed in Applicant's Related Art because it aids in increasing the breakdown voltage.

Additionally, since Merchant and Applicant's Related Art are both from the same field of endeavor, the purpose disclosed by Applicant's Related Art would have been recognized in the pertinent art of Merchant.

In regards to claims 5 and 9, Merchant discloses the following:

a) a field plate (7) formed over the top oxide layer, the first gate oxide (See Figure 1).

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In regards to claims 5 and 9, Merchant fails to disclose the following:

- a) a second gate oxide.

However, Applicant's Related Art discloses a second gate oxide (See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a second gate oxide as disclosed in Applicant's Related Art because it aids in increasing the breakdown voltage.

Additionally, since Merchant and Applicant's Related Art are both from the same field of endeavor, the purpose disclosed by Applicant's Related Art would have been recognized in the pertinent art of Merchant.

In regards to claims 7 and 11, Merchant fails to disclose the following:

- a) the first gate oxide has a length of approximately 3-4 μ m, and wherein the second gate oxide has a length of approximately 1-2 μ m.

However, the applicant has not established the critical nature of the dimension where the first gate oxide has a length of approximately 3-4 μ m, and wherein the second gate oxide has a length of approximately 1-2 μ m. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

In regards to claim 8, Merchant discloses the following:

- a) a buried oxide layer formed over a semiconductor substrate (See Figure 1);
- b) a silicon layer formed over the buried oxide layer, wherein the silicon layer comprises a source region, a body region, and a drift region (See Figure 1);
- c) a top oxide layer formed over the silicon layer (See Figure 1); and
- d) a first gate oxide formed over the silicon layer adjacent the top oxide layer (See Figure 1).

In regards to claim 8, Merchant discloses the following:

- a) the first gate oxide, top oxide layer and the body region (See Figure 1).

In regards to claim 8, Merchant fails to disclose the following:

- a) a second gate oxide.

However, Applicant's Related Art discloses a second gate oxide (See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a second gate oxide as disclosed in Applicant's Related Art because it aids in increasing breakdown voltage.

Additionally, since Merchant and Applicant's Related Art are both from the same field of endeavor, the purpose disclosed by Applicant's Related Art would have been recognized in the pertinent art of Merchant.

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9. Claims 6 and 10 are rejected under 35 U.S.C. 103(a) as obvious over Merchant (U.S. Patent No. 5,412,241) in view of Applicant's Related Art and Seeds et al. (U.S. Patent No. 3,936,858).

In regards to claims 6 and 10, Merchant discloses the following:

a) the first gate oxide has a thickness in a range of approximately 300-600A (See Column 2 Lines 39 and 40).

In regards to claims 6 and 10, Merchant fails to disclose the following:

a) a second gate oxide has a thickness in a range of approximately 900-1200A.

However, Seeds et al. ("Seeds") discloses a gate oxide that has a thickness around 1200A (See Column 8 Lines 52-55). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a gate oxide that has a thickness around 1200A as disclosed in Seeds because it aids in increasing the threshold voltage.

Additionally, the applicant has not established the critical nature of the dimension where the first gate oxide has a thickness in a range of approximately 300-600A, and wherein the second gate oxide has a thickness in a range of approximately 900-1200A. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

Finally, since Merchant and Seeds are both from the same field of endeavor, the purpose disclosed by Seeds would have been recognized in the pertinent art of Merchant.

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10. Claim 12, as far as understood, is rejected under 35 U.S.C. 103(a) as obvious over Merchant (U.S. Patent No. 5,412,241) in view of Applicant's Related Art, Seeds et al. (U.S. Patent No. 3,936,858) and Shirahata et al. (U.S. Publication No. 2002/0175380).

In regards to claim 12, Merchant fails to disclose the following:

a) a thickness of approximately 1200A for the second gate oxide results in an increase from approximately $1e^{12} \text{cm}^{-2}$ to approximately $2e^{12} \text{cm}^{-2}$ for a maximum allowable charge, and wherein a decrease of approximately 30% for a specific-on-resistance of the device.

However, Seeds et al. ("Seeds") discloses a gate oxide that has a thickness around 1200A (See Column 8 Lines 52-55). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a gate oxide that has a thickness in a range of approximately around 1200A as disclosed in Seeds because it aids in increasing the threshold voltage.

However, Shirahata et al. ("Shirahata") discloses a gate oxide that has various charges (See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a gate oxide that has a various charges as disclosed in Shirahata because it aids in increasing the threshold voltage.

Additionally, the applicant has not established the critical nature of the dimension where the first gate oxide has a thickness in a range of approximately 300-600A, and wherein the second gate oxide has a thickness in a range of approximately 900-1200A. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected

results relative to the prior art range.” *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

Finally, since Merchant, Seeds and Shirahata are both from the same field of endeavor, the purpose disclosed by Seeds and Shirahata would have been recognized in the pertinent art of Merchant.

Conclusion

11. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Merchant (U.S. Patent No. 5,362,979) discloses a SOI transistor with high performance; b) Gill et al. (U.S. Patent No. 5,420,060) discloses a floating gate memory array; c) Suzuki et al. (U.S. Patent No. 5,780,900) discloses a thin film silicon on insulator; d) Roisen et al. (U.S. Patent No. 5,893,729) discloses a SOI circuit for high voltage applications; e) Letavic et al. (U.S. Patent No. 5,973,341) discloses a thin film SOI device; f) Letavic et al. (U.S. Patent No. 6,028,337) discloses a thin film SOI device; g) Letavic et al. (U.S. Patent No. 6,127,703) discloses a thin film SOI device; h) Letavic et al. (U.S. Patent No. 6,133,591) discloses a SOI device; and i) Crowder et al. (U.S. Patent No. 6,372,559) discloses a double gate mosfet.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final

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communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

December 12, 2002



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